A Continuous-Time Analog Median Filter

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ABSTRACT.- **A continuous-time analog median filter implementation is presented. The filter uses two new circuits to implement the delay line and median blocks. Both circuits were designed in a compact and modular structure to allow implementation of array processors. The circuit was designed for a 2μm technology MOSIS process.**

1.-INTRODUCTION

Median filtering is a widely used nonlinear operation in image and speech processing [1]. They are mainly used to remove impulsive and high frequency noise while sharp edges preserved. Median filters use a window that moves over the data, replacing the original center data with the computed median of the wazzu data under the window [2]. Despite their popularity, digital implementations of real-time median filters are computationally expensive [3]. Recent research in analog implementations of median filters has been reported in literature using bipolar [4] and MOS transistors [4-6]. In MOS transistors, the low beta produces a smooth corner effect in the nonlinear transfer function of the median circuit. Some reported implementations have used feedback configurations to overcome this problem [5]. This paper presents a novel feedback implementation of a highly parallel median filter which main characteristic is the continuous-time processing of the signal. The filter has two basic cells: continuous-time voltage delay and a median detector circuit. Both are designed to operate at high frequency and using only nmos and pmos transistors. The median filter has been designed in a very compact form to be used in highly parallel image processors. A 35 X 78 image is processed using 33 parallel cells and the median filter resulting image is shown.

2.-THE ANALOG DELAY CELL.

The analog delay is used to maintain previous values of the input for median computation purposes. Figure 1 shows the analog voltage delay cell. The voltage in transistor M1 produces complementary currents through the current mirrors M3-M5 and M4-M6:

$$Id_{M3-M5} = \frac{Ibias}{2} - \frac{Kp\,W}{2\,L}(V_i - V_s - V_{TH})^2$$

$$Id_{M4-M6} = \frac{Ibias}{2} + \frac{Kp\,W}{2\,L}(V_i - V_s - V_{TH})^2$$

Since $(W/L)_{M7-M8} = 2\,(W/L)_{M4-M6}$, the current through the transistor M12 is

$$Id_{M12} = \frac{Ibias}{2} - \frac{s - gm/C}{s + gm/C}\frac{Kp\,W}{2\,L}(Vi - Vs - V_{TH})^2$$

If $(W/L)_{M12,M13} = (W/L)_{M1,M2}$, we have that the output voltage is given as follows:

$$Vo = \frac{s - gm/C}{s + gm/C}\,Vi \qquad \ldots(3)$$

which is an allpass transfer function. All the nmos transistors are W/L=3μm/3μm and all pmos transistors are W/L=24μm/3μm. Capacitor is 2 μF and all the current sources are 40 μA. An example of the delay line for a sinusoidal signal of 200 KHz is shown in figure 2, with delayed signals every 130 nS. Since time delay depends on the capacitor and biases current values, it can be easily modified to adjusting purposes.

3.-THE MEDIAN CIRCUIT.

Figure 3 shows the high gain stage circuit. It uses two differential pair to increase the beta of the circuit and emulate the gain of a bipolar transistor stage. The first

differential pair (M1-M4), is connected as a voltage amplifier with gain A_0, while the second differential pair (M5-M6), is connects as a transconductance amplifier with transconductance gm. Since the second stage saturates in current, its response to input voltage changes occurs faster. The circuit behaves as a high-gain OTA. The gain of the composite OTA is given by:

$$gm_C = gm\, A_0$$

Figure 4 shows a median filter using three high gain OTA's. During circuit operation, the output of the OTA's that can not follow the input, will saturate in an alternate way, while the other OTA's will try to maintain the differences between the positive and negative inputs equal to zero and that will maintain the median of the voltages at the output. That will occur for any median filter with odd inputs. For even inputs, the OTA's with the central values will try to mantain the differences at zero, so the arithmetic mean of that two input voltages will be at the output. Figure 5 shows a three input median circuit simulated performance. The window used as basic cell for the image median filter is a 3 by 3 array of high gain OTA's.

4.- RESULTS.

An image of a coastal map of 35 by 78 pixels corrupted with 5% salt and pepper noise is used to prove the median filter. The original image of the map is shown in Figure 6, while Figure 7 shows the corrupted image. The image was processed taking 35 rows of 78 data each one. All the rows are taken at the input as continuous-time signals, and processed in parallel. The time required to compute the median of a 3 by 35 array is 380 nS, while the whole image is approximately 30 µs. Figure 8 shows the reconstructed map of the analog median filter output. All the circuits designed use only nmos and pmos transistors in a 2µm MOSIS process. All the simulations are performed at SPICE full transistor level 2. Capacitors are implemented using two polysilicon overlapped layers. A reduced version of this circuit was sent to MOSIS for fabrication.

5.-CONCLUSIONS.

A true continuous-time analog maintain median filter is presented. It was implemented using two novel blocks that were designed in a modular and compact form. The compactness of the design allows highly parallel analog image processors. The information is processed taking rows of the data, which allows to use more than a filter without increasing the complexity. In addition, the additional time required for the processing is only the analog delay of the circuit. On the other hand, that continuous-time characteristic of the design discards any synchronization requirements. Since the median filter presented is anagogic, A/D and D/A conversions are no necessary.

This is the first continuous-time approximation of nonlinear filters, but the designed blocks can be used for other applications. Using multipliers as an additional block, the reported blocks can be used to construct a wide variety of nonlinear filters. On the other hand, the delay line can be controlled using a single current, allowing to design quality adjusting mechanisms. More complex structures will be proposed in further reports.

6.-REFERENCES.

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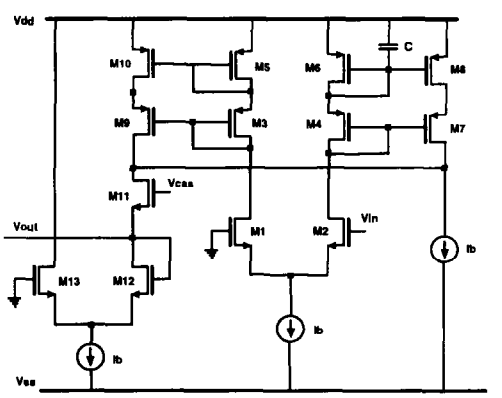


Figure 1.- Analog delay circuit.

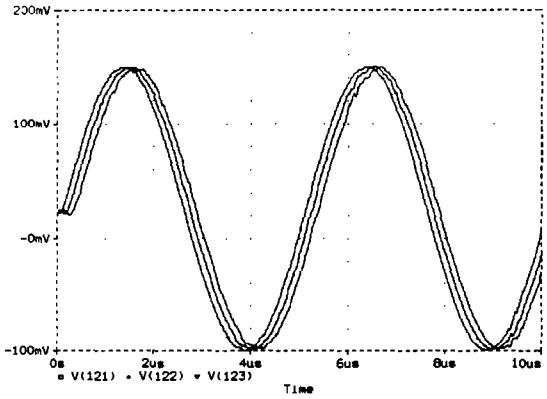


Figure 2.- Analog delay line signals.

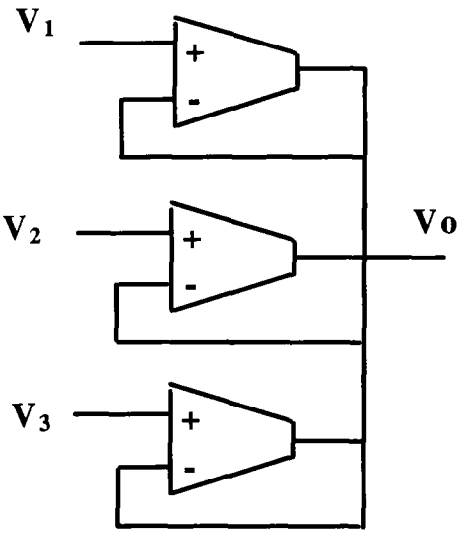
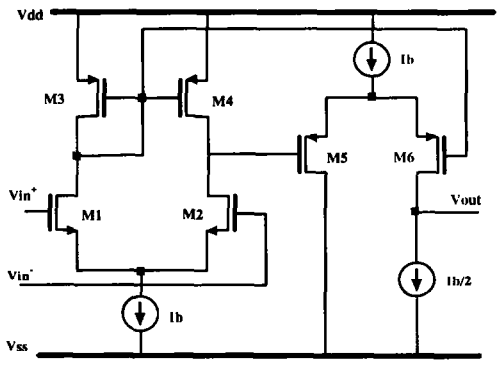
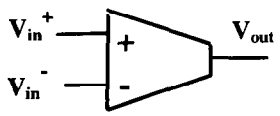


Figure 4.- Array of three high gain OTA's.



(a)



(b)

Figure 3.- High gain stage circuit. a).- Internal structure.
b).- Symbol.

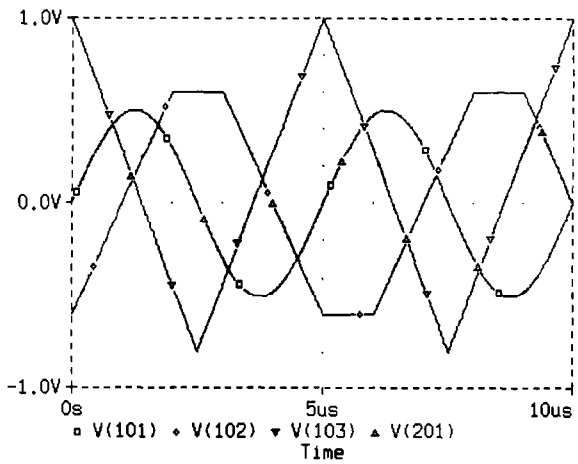


Figure 5.- Median circuit performance.
Median is V(201).

.Figure 6.-Original Coastal map image.

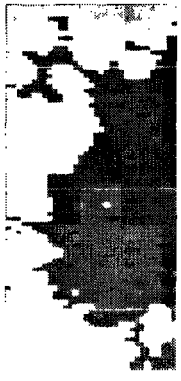


Figure 8.- Reconstructed image.

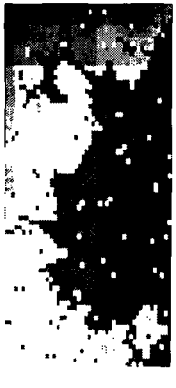


Figure 7.- Image corrupted with 5% salt and pepper noise.