

VLSI Cellular Neural Network Based Median Filter for Real-Time Video Signal Processing

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1. Introduction

An increasing demands for video application in teleconferencing, multimedia services, autonomous navigation, motion analysis, object tracking, surveillance, astronomical, and medical imaging make high rigorous requirements for real-time noise filtering algorithms to improve the visual quality and the performance of subsequent processing tasks such as coding, analysis and interpretation. Median based filters - as it was well reported in literature - belong to the class of nonlinear filters and are very useful for these applications. This is because of two intrinsic properties of median filters: edge preservation while reducing efficiently the noise. Even though the theory and computer simulation of median filters are widely studied in the literature [1], the hardware implementation problem still presents opened questions. In VLSI CMOS implementation two concepts are considered: digital [2] and analog [3]. Digital approach (using DSP or FPGA) is very accurate, however is time-consuming and occupies large silicon area which makes this concept expensive for today needs of real-time applications. In comparison with this approach an analog version seems to be much more economic, and even though it is not so accurate as digital one, it can be accepted for many applications. Therefore, the problem of

analog realizations of median filters is worth to study in details.

2. Main idea of the paper

Generally, the function performed by the median filter, according to its mathematical definition, is to apply a two dimensional window (rectangular, hexagonal, cross, and other shape) of given size to a group of pixels surrounding the center-positioned pixel for which the filter function is performed. The pixel values are sorted in ascending order and the “median” value, i.e. the sample laying just in the middle position of the ascending staircase is assigned to the center pixel as a filter response. Next, the window is shifted one position in horizontal and/or vertical direction of the image and the operation is repeated on the new set of pixels laying within the window. This algorithm is rather easy to implement in digital systems but, as was mentioned above, it costs time and chip area. The median function however, can be realized also in continuous-time fashion using signals like currents and/or voltages in resistive grid circuits [3]. In this paper the VLSI CMOS implementation of analog median image filter based on Cellular Neural Network (CNN) technique [4] is presented.

In general, CNN is 1-, 2-, or 3 - dimension array of nonlinear analog

processors (cells), connected locally by signal interactions. The connectivity is spatially-invariant, therefore the mathematical model and the functioning of the whole CNN is reduced to the model of its one cell. The system is dynamical one with two sources of input excitation (constant input signal and initial condition for storage element - capacitor of each cell). Given input signals at the initialization moment, the CNN resolves in time to its transient state going to one of its stable points. Parameters of the cell are: weights values of feedback and forward interactions within the frame of well defined neighborhood. These parameters determine various functions of real-time signal (image) processing performed by CNN. In original version the CNN is realized with electronic linear and nonlinear voltage-controlled current sources with gain parameters playing the role of weight values. It will be shown in the paper that for realization of median filtering in CNN the cell model is composed of forward weights only, implemented by nonlinear resistors of hard-limiting current-voltage characteristics.

The block scheme of the filter operating with standard video signal in real time is presented in Fig.1. The chip was implemented in VLSI 2 μm CMOS technology and consists of 1-D CNN processor with $N=64$ cells. Filtering window is 3x3 pixel size. Median filtering is processed on the content of three actual video lines. Each line, which is composed of N pixels is sampled and stored sequentially in the temporal analog

memory SH. This step is controlled by separated synchronous signal S and clock signal Clk shifted in the register SR. After loading current video line the content of SH is written parallelly to 3xN operation analog memory AM followed by new lines are loaded to the SH. When analog memory AM is fully loaded by pixel content of three consecutive lines, the median parallel filtering begins in the CNN 1xN array. The filtering results of each pixel is sent in real time to video output. All the electronic circuitry was based on OTA and current-mode analog technique and designed using SPICE software and Cadence platform. The final chip consists of about 12000 MOS transistors occupying about 5 mm^2 silicon die. Test results of the chip will be presented in the conference communication.

References

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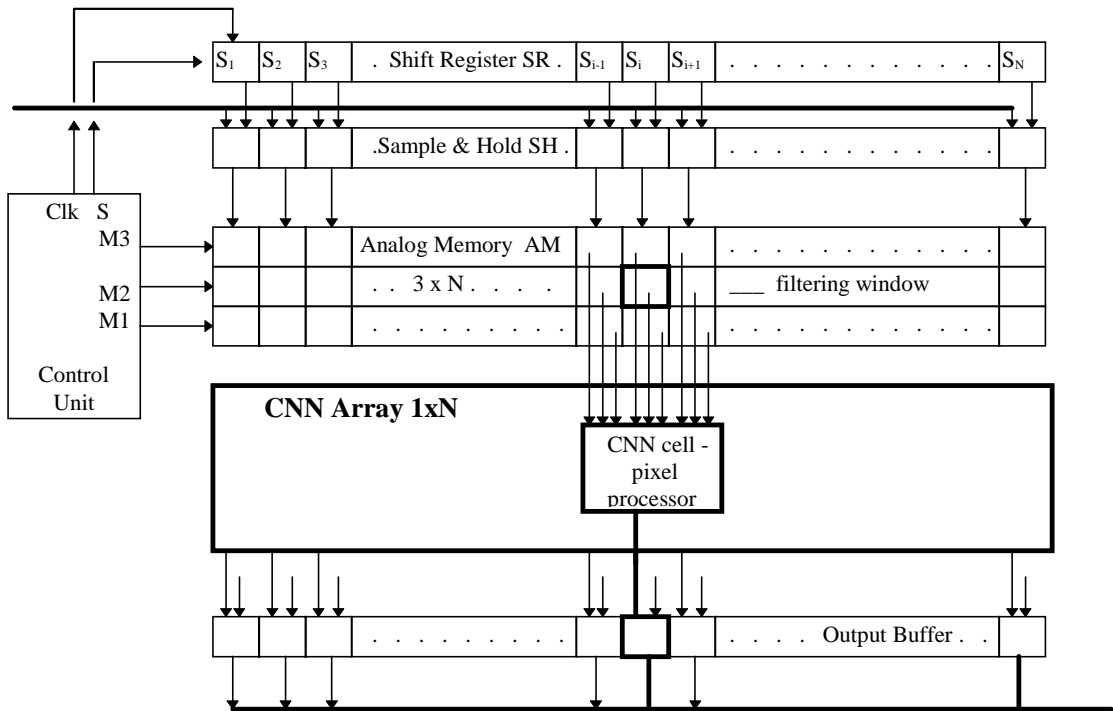


Fig. 1 Block scheme of CNN-based median filter for real-time video signal processing